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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, THAN VINH	
ART UNIT	**PAPER NUMBER**
2187	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/053,340	WARE ET AL.	
	Examiner	Art Unit	
	Than Nguyen	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,6,9,11,13,14,16-19,21,23-25 and 27-36* is/are rejected.

7)☒ Claim(s) *3,4,7,8,10,12,15,20,22 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/16/07, 12/5/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 8/16/07 has been entered.

2. Claims 1-36 are pending.

3. The IDSes, filed 8/16/07 and 12/5/07, have been considered.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1,2,5,6,18,19,21,23,24,30,31,34,35 are rejected under 35 U.S.C. 102(e) as being anticipated by Vogley (US 5,615,358).

As to claim 1:

6. Vogley teaches a memory system comprising: a first memory controller (skewing circuit 26; Fig .1 or sync controller logic; Fig. 10); a first memory component (SMD 30; a first address and control bus (address/control bus 27/60) connected to the first memory controller and the first memory component, the first address and control bus including a plurality of signal conductors that extend from the first memory to the first memory component (Fig. 1); and a first data bus (data bus 28) connected to the first memory controller and to the first memory, wherein the first data bus uses differential signaling and has a first data bus symbol time that is shorter than a first address and control bus symbol time of the first address and control bus (data bus has different delay/symbol time than address/control bus; delayed signals generated by 26; 4/38-54).

As to claim 2,6,19:

7. Vogley teaches a second memory component connected to the first address and control bus and to the first data bus (SMD 30; Fig. 1).

As to claim 5:

8. Vogley teaches a memory system comprising: a first memory controller (skewing circuit 26); a first memory component (SMD 30); a first address and control bus (address/command bus 27/60) connected to the first memory controller and to the first memory component, the first address and control bus including a plurality of signal conductors that extend from the first memory to the first memory component (Fig. 1); a first clock signal conductor (clock 29) connected to the first memory controller and to the first memory component; and a first data bus (data bus 28) connected to the first memory

controller and to the first memory component, wherein the first data bus has a first data bus symbol time that is shorter than a first address and control bus symbol time of the first address and control bus and wherein the first address and control bus symbol time is shorter than a first clock signal cycle time of the first clock signal (data bus has different delay/symbol time than address/control bus; delayed signals generated by 26; 4/38-54).

As to claim 18:

9. Vogley teaches a memory system comprising: a first memory controller (skewing circuit 26); a first memory component (SMD 30); a first address and control bus (address/control bus 27/60) connected to the first memory controller and to the first memory component, the first address and control bus including a plurality of signal conductors that extend from the first memory to the first memory component (Fig. 1); and a first data bus (data bus 28) connected to the first memory controller and to the first memory component; wherein the first data bus uses differential signaling and wherein the first memory component accesses a first word stored in the first memory component, the first word being wider than a first data bus width of the first data bus (data bus can send data of varying length/size; cols 3-4)

As to claim 21:

10. Vogley teaches a memory system comprising: a first memory controller (skew circuit 26); a first memory component (SMD 30); a first address and control bus (address/control bus 27, 60) connected to the first memory controller and to the first memory component, the first address and control bus including a plurality of signal

conductors that extend from the first memory to the first memory component (Fig. 1); and a first data bus (data bus 28) connected to the first memory controller and to the first memory component, wherein the first memory controller includes a first receive circuit having a first read timing adjustment subcircuit for adjusting a first adjustable read data sampling time point for first read data sampled from the first data bus and wherein the first data bus uses differential signaling (skewing circuit adjust timing delays/samples; 4/38-54).

As to claim 23:

11. Vogley teaches a calibration process is used to adjust a first termination value of the first termination structure (termination module(s) adjusted according to memory installed; 3/65-4/24).

As to claim 24:

12. Vogley teaches the first memory controller contains a first transmit circuit having a first write timing adjustment subcircuit for adjusting a first adjustable write data driving time point for first write data driven on the first data bus (Fig. 3; timing control 42).

As to claims 30,31,34,35:

13. Vogley teaches a memory module having the first memory component and plurality of signal conductors disposed therein (SMD 30; Fig. 1).

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 9,11,13,14,16,17,25,27,28,29,32,33,36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vogley (US 5,615,358) in view of Sanwo et al (US 5,530,623).

As to claim 9,11,14,16,25,29:

16. Vogley teaches a memory system comprising: a first memory controller (skewing circuit 26); a first memory component (SMD 30); a first address and control bus (address/control bus 27/60) connected to the first memory controller and to the first memory component, the first address and control bus including a plurality of signal conductors that extend from the first memory to the first memory component (Fig. 1); and a first data bus (data bus 28) connected to the first memory controller and to the first memory component, wherein the first data bus has a first data bus symbol time that is shorter than a first address and control symbol time of the first address and control bus (data bus has different delay/symbol time than address/control bus; delayed signals generated by 26; 4/38-54). Vogley does not specifically teach the first memory component includes a first termination structure connected to the first data bus. It is well-known to use a terminal structure to a memory module to match the impedance of the memory device and its lines. Sanwo et al teaches using termination structure attached to a memory module to match the impedance of the memory device (4/11-37). Thus, it

would have been obvious to one of ordinary skills at the time of the invention to attach terminal structure(s) to the memory modules 30 of Vogley, as suggested by Sanwo.

As to claim 13,17,27:

17. Vogley teaches a calibration process is used to adjust a first termination value of the first termination structure (termination module(s) adjusted according to memory installed; 3/65-4/24).

As to claim 28:

18. Vogley teaches the first memory controller contains a first transmit circuit having a first write timing adjustment subcircuit for adjusting a first adjustable write data driving time point for first write data driven on the first data bus (Fig. 3; timing control 42).

As to claims 32,33,36:

19. Vogley teaches a memory module having the first memory component and plurality of signal conductors disposed therein (SMD 30; Fig. 1).

Allowable Subject Matter

20. Claims 3,4,7, 8,10,12,15,20,22,26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

21. As to claim 3,7,20, the prior art does not further teach a second memory component connected to the first address and control bus; and a second data bus connected to the first memory controller and to the second memory component, wherein

the second data bus uses differential signaling and has a second data bus symbol time that is shorter than the first address and control bus symbol time of the first address and control bus.

22. As to claim 4,8,12 the prior art does not further teach wherein a quotient of the first data bus symbol time divided by the first address and control bus symbol time is less than or equal to 1/8.

23. As to claim 10,15 the prior art does not further teach a second memory component connected to the first address and control bus; and a second data bus connected to the first memory controller and to the second memory component, wherein the second memory component includes a second termination structure connected to the second data bus and wherein the first data bus symbol time is shorter than the first address and control bus symbol time of the first address and control bus.

24. As to claim 22, the prior art does not further teach a second memory component connected to the first address and control bus; and a second data bus connected the first memory controller and to the second memory component, wherein the first memory controller includes a second receive circuit having a second read timing adjustment subcircuit for adjusting a second adjustable read data sampling time point for second read data sampled from the second data bus and wherein the second data bus uses differential signaling.

25. As to claim 26, the prior art does not further teach a second memory component connected to the first address and control bus; and a second data bus connected to the first

memory controller and to the second memory component, wherein the first memory controller includes a second receive circuit having a second read timing adjustment subcircuit for adjusting a second adjustable read data sampling time point for second read data sampled from the second data bus and wherein the second memory component includes a second termination structure connected to the second data bus.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Than Nguyen whose telephone number is 571-272-4198. The examiner can normally be reached on 8am-3pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Than Nguyen can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Than Nguyen
Primary Examiner

Art Unit 2187